



SSC P485
Hardware Design Reference



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Intellon SSC P485 Hardware Design Reference

1. Introduction

The Intellon SSC P485 PL Transceiver IC is a highly integrated spread spectrum communication transceiver for use in low-cost networking applications. Features of the SSC P485 include:

- Physical Layer Transceiver
- Spread Spectrum Carrier™ Communication Technology
- 9600 Baud Data Rate
- Simple Host Interface
- Low Power Operation
- Minimal External Components Required
- 20 Pin SOIC Package

This document will focus on application of the SSC P485 in DC power line applications. Additional notes will be provided to assist the designer in application of the P485 in other low-cost network environments.

2. Application Overview

A typical network node based on the SSC P485 PL Transceiver IC is diagrammed in Figure 1. The Host System microcontroller interprets commands and data for a user application and provides the upper layers (Application, Network and Data Link) of the system communication protocol. Physical Layer services of the communication protocol are provided by the SSC P485 IC. Input and output signal amplification and filtering, coupling of the node to the communication medium and power functions are performed using external circuitry.

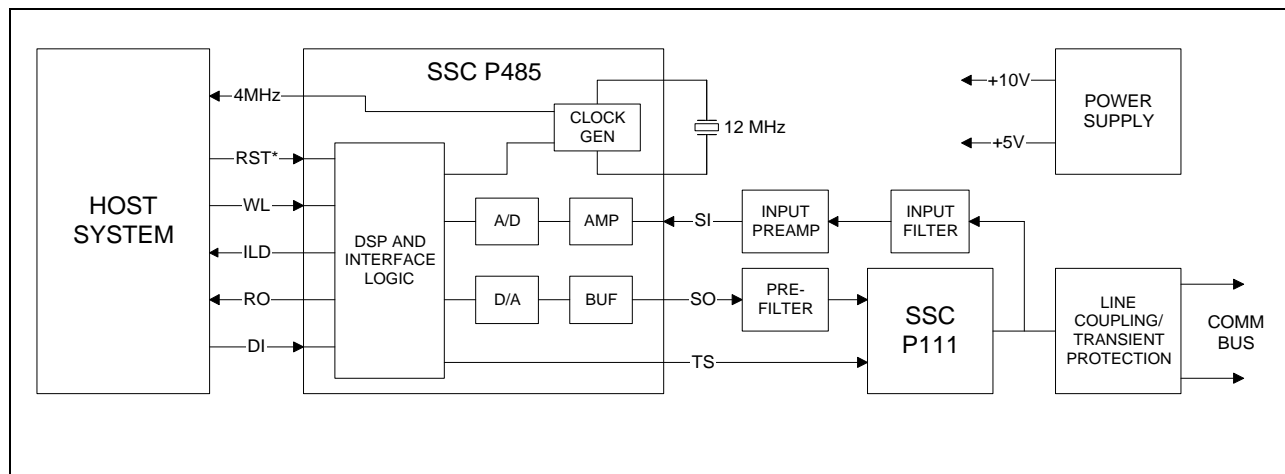


Figure 1. Typical SSC P485 Network Node

2.1 SSC P485 Host Interface

SSC P485 interface to the host system is supported through six signal lines. The Driver Input (DI) and Receiver Output (RO) lines allow data bits to be transferred to or from the SSC P485. Idle Line Detect (ILD) provides the host with the status of the communication medium. The Word Length (WL) input to the P485 allows the host to select 10-bit frames (START, eight data bits, STOP) or 11-bit frames (START, nine data bits, STOP) for message transfers. The P485 defaults to 10-bit frames if the WL pin is pulled to +5V or left unconnected. The active-low Reset (RST*) signal to the P485 is supplied by the host. An optional 4 MHz Clock Output (4MHz) is provided by the P485 as a host clock source. All host interface signals are TTL level compatible. The protocol used for SSC P485 communication with the host is defined by the user.

2.2 SSC P485 Medium Interface

Analog data is transferred between the communication medium (DC power line, twisted pair cable, etc.) and the SSC P485 over the Signal In (SI) and Signal Out (SO) pins. In transmit mode, SSC “chirps” from the P485 SO pin are routed through a low-pass Pre-filter to remove high-frequency energy from the transmit signal and then to the SSC P111 output amplifier. The P111 is enabled by the SSC P485 Tri-State (TS) signal. Once amplified, the output signal passes to the communication medium through the Line Coupling/Transient Protection circuit.

In receive mode, the analog communication signal passes through the Line Coupling circuit to the Input Filter. This bandpass filter passes the chirp frequency band (100 to 400 kHz) and rejects out-of-band noise signals. Additional signal gain is provided by the Input Preamp. The amplified and filtered input signal is then applied to the SSC P485 SI input.

3. SSC P485 Functional Description

The functional blocks of the SSC P485 PL Transceiver IC are shown in the SSC P485 “box” in Figure 1. The analog communication signal enters the SSC P485 at the SI signal pin and is amplified by the buffer amplifier (Amp). The amplified signal is then passed to the one-bit Analog/Digital converter (A/D) in preparation for digital signal processing of the signal.

Digital signal processing of the input signal includes detection of the SSC “chirp” waveform using a matched-filter correlator and tracking of the acquired signal. Signal state information is passed from the DSP circuitry to the Interface Logic for message decoding and transmission to the Host.

Messages to be transmitted are transferred from the Host to the P485 Interface Logic. Symbols are then passed to the DSP block, which generates the Spread Spectrum Carrier superior and inferior states using a ROM look-up table. The table values drive an 8-bit Digital-to-Analog converter, producing the SSC “chirp” analog waveform. This waveform is buffered and output at the SO pin when the Tri-State signal is set high.

4. SSC P485 Power Line Node Application Example

Figure 2 is a schematic of a typical power line node based on the SSC P485. This node provides the required interface circuitry between the SSC P485 and a DC power line. Detailed descriptions of this circuit follow.

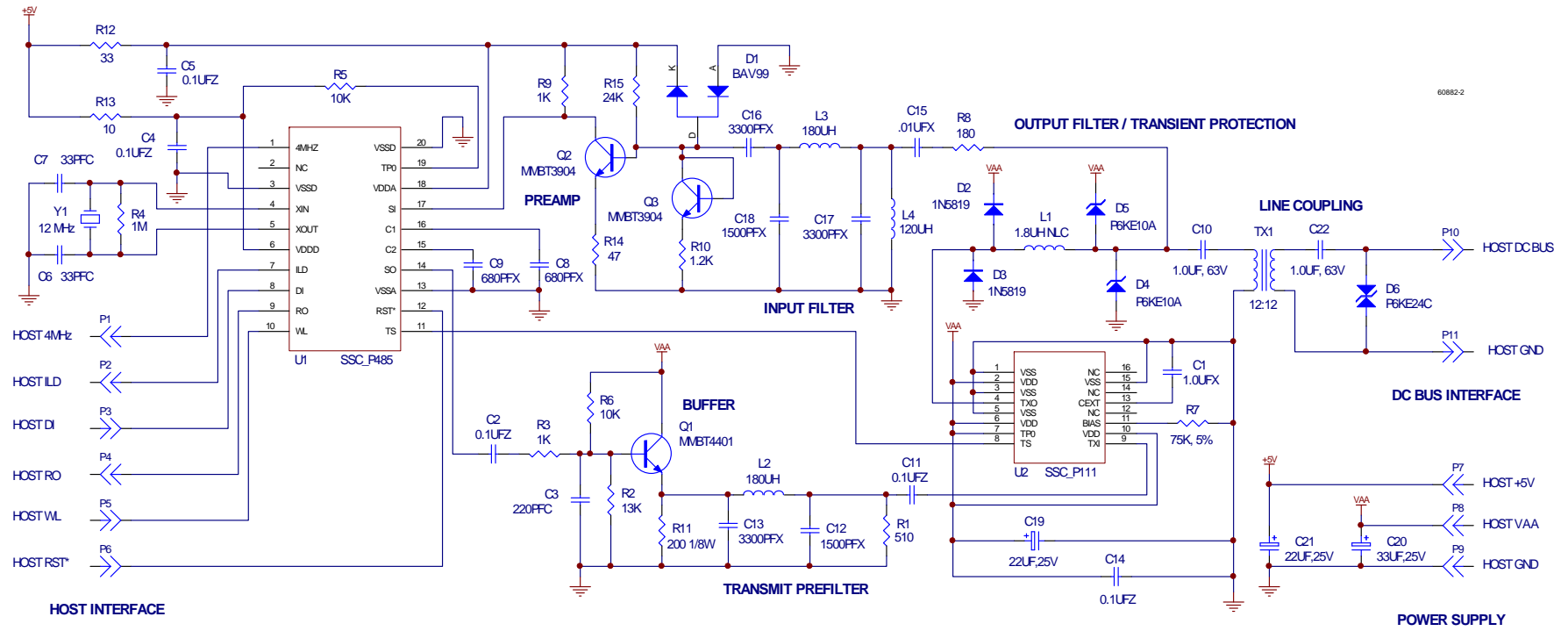


Figure 2. P485 Reference Design

4.1 Power Line Coupling

4.1.1 Description

Transformer TX1, capacitor C22 and transient surge suppressor D6 illustrate a typical 12 VDC power line coupling circuit for use with the SSC P485. The transformer provides a linear transfer function for the 100-400 kHz Spread Spectrum Carrier signal. Capacitor C22 limits low frequency noise and blocks the power line DC level from the transformer secondary. D6 provides protection against high voltage transients on the power line.

4.1.2 Coupling Transformer Specification

The toroidal coupling transformer used in the reference design has the following specifications:

Core:	Phillips #204T250 / 3C81
Wire:	#28 AWG Insulated (Teflon)
Breakdown Voltage:	1500 VAC, 60 Hz, 1 Minute
Winding:	1:1 Turns Ratio, 12 Turns Primary and Secondary
Inductance:	0.25 mH (Approx)

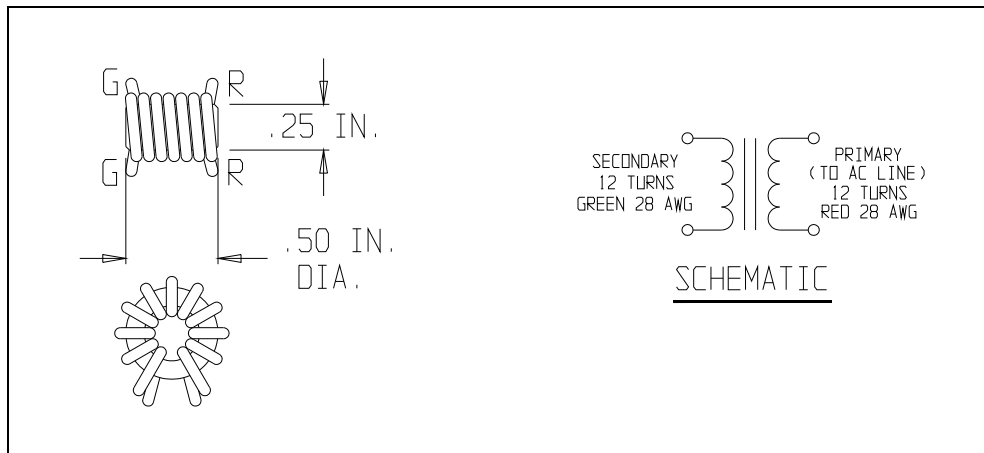


Figure 3. Coupling Transformer Specification

Transformers meeting these specifications are available from:

JML ENGINEERING

JMLENG@AOL.COM

1-954-609-9281

4.2 Receive Input Filter

The SSC P485 requires an external bandpass input filter to attenuate strong out-of-band frequencies. The recommended filter is a passive 6-pole LC configuration and is made up of R8, C15, L4, C17, L3, C18 and C16 in Figure 2. Specifications for the filter are listed in Table 1.

Table 1. Input Filter Response

Response	F(low)	F(high)
- 3 dB	100 kHz	400 kHz
- 30 dB	40 kHz	1.0 MHz

4.3 Receive Preamp

The filtered input signal is buffered to the SSC P485 by a transistor amplifier made up of Q2, Q3, R9, R15, R14, R10 and D1. The amplifier provides 20 dB of signal gain. This value is chosen to provide node sensitivity of 1 mV peak-to-peak. Additional gain will increase the sensitivity of the node but may reduce noise immunity.

Resistors R10 and R15 set the DC bias point for the amplifier, placing the DC level of the SSC P485 SI input to mid-supply. R10 and R15 also serve to terminate the receive input filter at approximately 900 ohms. Diode-connected transistor Q3 serves to stabilize the amplifier's DC bias point as a function of ambient temperature. The dual diode package, D1, clamps the signal applied to the SSC P485 SI pin to the power supply range of the device. This provides additional transient protection for the SSC P485.

4.4 Transmit Mode Circuitry

The application circuit of Figure 2 utilizes the Intellon SSC P111 PL Media Interface IC for amplification of the SSC signal applied to the power line. In the transmit mode, the SSC P485 internally generates the SSC "chirp" waveform using a ROM look-up table and an 8-bit digital-to-analog converter. Since this signal is digitally generated, it is necessary to filter the output to remove high-frequency components. The signal from the P485 SO (Signal Output) pin is first AC coupled through C2 to a single-pole low-pass filter consisting of R3 and C3. The signal is further filtered by a 3-pole low-pass filter made up of C13, C12, L2 and R1. This filter requires a low drive impedance so the signal is buffered by the emitter follower made up of Q1, R6, R2 and R11. Filtering of the chirp signal is provided to ensure compliance with recommended practices on power line conducted emissions. The distortion and noise amplitude at the output of the node must be less than 1 mV RMS in the AM broadcast frequency range, 535 to 1705 kHz, to meet SAE J1113/41 requirements.

After pre-filtering, the chirp signal is AC coupled through C11 into the SSC P111 Power Amplifier input pin, TXI. The Power Amplifier increases the voltage amplitude of the signal by a factor of 2. The signal then exits the SSC P111 IC TXO pin and is filtered by inductor L1. The resulting signal is AC coupled through C10 to the Power Line Coupling Circuitry and applied to the power line.

If the P111 is operated into line impedances less than 1 to 2 ohms, clipping of the output signal may occur for high output levels. In these applications, it may be necessary to reduce the output signal voltage to maintain acceptable output distortion levels. The output signal voltage may be reduced in the application circuit by varying the ratio of the voltage divider made up of resistor R3 and the parallel combination of resistors R2 and R6.

4.5 Additional Requirements and Considerations

4.5.1 Clock Interface

The SSC P485 Crystal Output (XOUT) and Crystal Input (XIN) pins connect the on-chip Pierce oscillator to an external 12 MHz crystal. Additional components required include a 1 megohm resistor, R4, in parallel with the crystal Y1 and a 33 pF (nominal) capacitor from each crystal pin connection to ground. The value of capacitors C6 and C7 may require experimentation (± 10 pF) to compensate for printed circuit layout trace capacitance.

The crystal used with this circuit should be an "AT cut" device rated for 1 mW minimum. ESR of the device should be less than 100 ohms. Frequency tolerance is ± 100 PPM over the expected temperature range of the SSC P485 node device.

The SSC P485 also provides a 4 MHz clock output signal for use by a host microcontroller or other support circuitry. This signal is intended to drive standard TTL loads and will sink up to 2 milliamps. In special applications, termination of the 4 MHz clock output may be necessary to improve clock signal quality. The characteristics of the driven load will determine the type of termination used. If source termination is required, a 33 ohm resistor should be used in series with the 4 MHz output. This resistor should be located as close as possible to the P485 clock output pin. In applications requiring termination at the input to the driven device, the recommended termination is a series resistor of 100 ohms followed by a shunt capacitance of 100 pF, located near the driven circuit pin.

4.5.2 Power Supply

The circuit shown in Figure 2 requires two external power sources. A regulated +5 VDC $\pm 10\%$ power source at 20 mA (typical) is required for the SSC P485 IC. A regulated supply of +10 VDC $\pm 10\%$ at 250 mA (minimum during transmit) is necessary for the P111 Output Amplifier.

The digital (VDDD) and analog (VDDA) power supplies of the SSC P485 should be isolated and filtered to minimize leakage of noise from the digital portion of the IC to the analog circuitry. Filter R12/C5 performs this isolation for the SSC P485 analog power supply (VDDA) and filter R13/C4 performs this function for the digital supply (VDDD). The transistor buffer circuit, Q2, is also powered from the "VDDA" supply to minimize noise coupling into the SSC P485 SI input. R12 and R13 are chosen to provide the required isolation with minimal drop of the SSC P485 supply voltages.

The SSC P111 Technical Data Sheet specifies that the IC may be operated over a power supply voltage range of 9 to 11 VDC. This supply range ensures that the IC will operate at full signal output of 6 Vp-p without excessive dissipation in the IC's output transistors or unacceptable distortion in the output signal. System reliability will be enhanced if the supply voltage is 10 VDC or less. If necessary, the P111 will provide output signal levels up to 6 Vp-p at supply voltages down to 8 VDC with only a slight increase in output distortion.

Note that the power rating of the +10 Volt supply will depend on the transmit duty cycle of the node. In applications where a +10 Volt supply capable of supplying 3 to 4 watts continuously is not possible, it may be necessary to limit the transmit duty cycle and use a "storage capacitor" to supply the instantaneous current necessary for transmission of each message.

4.5.3 Operating Temperature

The SSC P485 and SSC P111 are designed to operate over the temperature range from - 40 to + 85 C. Typical power line communication applications require message transmit duty cycles of less than 10% and internal heating of the IC's should not be a problem. In applications where higher transmit duty cycles will be utilized, the SSC P111 PL Media Interface IC is designed to reduce its signal gain when the on-chip temperature reaches a pre-determined level. This action reduces power dissipated in the output transistors so that permanent damage does not occur.

4.5.4 Layout Considerations

The SSC P485 node application operates with millivolt-range signals at low RF frequencies. Careful PC board layout is important. Bypassing of the SSC P485 power supplies should be performed as near as possible to the IC pins. Analog signal ground traces should be physically separated from the analog power traces and digital grounds. The ground traces should be tied together at only one point.

All system clock sources should be placed as far as possible from the analog input circuitry of the P485, and if possible, ground plane should be placed between these circuits. Ground plane should also be used to isolate the low-level analog circuitry from on-board digital circuitry.

4.5.5 Construction Practices

The SSC P485 reference design described in this note specifies the use of surface-mount construction techniques. These techniques may not be appropriate for devices that will be subjected to high mechanical vibration or shock levels. Though-hole construction techniques may be used in P485 applications as long as the circuit board layout considerations described in this note are applied.

4.5.6 SSC P111 Transient Protection

The SSC P111 typically drives a DC power line. Voltage transients present on the line will conduct back through the coupling circuitry and onto the SSC P111 output pin. Under certain conditions, transients with high amplitudes and/or fast rise times can damage the SSC P111 IC. Transient suppression circuitry is required to ensure proper operation of the SSC P111 IC. The recommended protection circuitry includes a Metal Oxide Varistor (MOV), Transient Voltage Suppressor (TVS) or Zener Diode combination at the DC Power Line Coupler, and a TVS/Schottky Diode combination at the SSC P111 IC output pin. The TVSs should be placed between the output filter inductor and capacitor, as shown in Figure 2. This isolates the capacitance of the TVSs (via the inductor) from the SSC P111 output, maintaining required phase margin. The TVSs should be selected based on the power supply voltage (VAA) used to provide power to the SSC P111. The TVSs must turn on before the transient amplitude reaches the rails of the power supply, while still allowing the SSC “chirps” to pass by the TVSs unattenuated.

Note: Substituting slower transient protection devices may result in reduced transient protection. Refer to Application Note #0071, Surge Protection Techniques for Power Line Communications, for further information on selection of transient protection devices.

Recommended TVSs based on the power supply voltage used are listed in the table below.

Maximum Power Supply Voltage (VAA)	Transient Voltage Suppressors
9 VDC	P6KE9.1A
10 VDC	P6KE10A
11 VDC	P6KE11A

Keep in mind that these recommendations may not be sufficient for all applications and that environments with high voltage transient activity may require additional protection elements.

5. SSC P485 Power Line Node Bill-of-Materials

The following BOM lists recommended components for the Intellon SSC P485 Reference Design shown in Figure 2.

ITEM	PART NO	PART DESCRIPTION	QTY	REF DESIG	MFR
1		SCHEMATIC, P485/P111 REFERENCE DESIGN	1		INTELLON
2					
3					
4					
5					
6	C0603Z5U250-104MNE	.1 UF 25V 20% Z5U 0603 CAP CER SMT	5	C2, C4, C5, C11, C14	VENKEL
7	C0603X7R250-103KNE	.01 UF 25V 10% X7R 0603 CAP CER SMT	1	C15	VENKEL
8	GMC31X7R105K25NE	1.0 UF 25V 10% X7R 1206 CAP CER SMT	1	C1	CAL-CHIP
9	ECQ-V1J105JM	1.0 UF 63V 5% RADL CAP METAL FILM	2	C10, C22	PANA
10	TA025TMC226MDR	22 UF 25V 20% D-CS CAP TANT SMT	1	C19	PANA
11	C0603COG500-330JNE	33 PF 50V 5% COG 0603 CAP CER SMT	2	C6, C7	VENKEL
12	C0603X7R500-332KNE	3300 PF 50V 10% X7R 0603 CAP CER SMT	3	C13, C16, C17	VENKEL
13	C0603X7R500-152KNE	1500 PF 50V 10% X7R 0603 CAP CER SMT	2	C12, C18	VENKEL
14	C0805COG500-681JNE	680 PF 50V 5% COG 0805 CAP CER SMT	2	C8, C9	VENKEL
15	C0603COG500-221JNE	220 PF 50V 5% COG 0603 CAP CER SMT	1	C3	VENKEL
16	EEV-HB1E220P	22 UF 25V 20% 105c D-CS (HB) CAP ALUM ELEC.	1	C21	PANA
17	EEV-HB1E330P	33 UF 25V 20% 105c D-CS (HB) CAP ALUM ELEC.	1	C20	PANA
18					
19	BAV99	200 MA 70 VOLT DUAL HIGH SPEED SWITCHING DIODE SOT-23	1	D1	DIODES
20	P6KE10AGI	10 VOLT 600W UNIDIRECTIONAL TVS DO-15	2	D4, D5	GEN / INST
21	P6KE24CAGI	24 VOLT 600W BIDIRECTIONAL TVS DO-15	1	D6	GEN / INST
22	1N5819	40V 1 AMP SCHOTTKY RECT CASE 59-04	2	D2, D3	MOTO
23					
24	NLC453232T-1R8K	1.8 UH 10% 1812 900 MA LARGE CURRENT IND SMT	1	L1	TDK
25	NL322522T-181J	180 UH 5% 1210 60 MA IND SMT	2	L2, L3	TDK
26	NL322522T-121J	120 UH 5% 1210 70 MA IND SMT	1	L4	TDK
27					
28	MMBT3904LT1	NPN EPITAXIAL SILICON G/P TRANSISTOR SOT-23	2	Q2, Q3	MOTO
29	MMBT4401	NPN EPITAXIAL SILICON SMALL SIGNAL TRANSISTOR SOT-23	1	Q1	DIODES INC
30					
31	RM06J133CT	13 K 5% 1/6W 0603 RES SMT	1	R2	CAL-CHIP

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ITEM	PART NO	PART DESCRIPTION	QTY	REF DESIG	MFR
32	CR0603-16W-470JT	47 OHM 5% 1/16W 0603 RES SMT	1	R14	VENKEL
33	RM06J105CT	1 MEG 5% 1/6W 0603 RES SMT	1	R4	CAL-CHIP
34	CR0603-16W-511JT	510 OHM 5% 1/16W 0603 RES SMT	1	R1	VENKEL
35	RM06J103CT	10 K 5% 1/16W 0603 RES SMT	2	R5, R6	VENKEL
36	CR0603-16W-753JT	75 K 5% 1/16W 0603 RES SMT	1	R7	VENKEL
37	RM06J181CT	180 OHM 5% 1/16W 0603 RES SMT	1	R8	CAL-CHIP
38	CR0603-16W-122JT	1.2 K 5% 1/6W 0603 RES SMT	1	R10	VENKEL
39	CR0603-16W-100JT	10 OHM 5% 1/16W 0603 RES SMT	1	R13	VENKEL
40	CR1206-8W-201JT	200 OHM 5% 1/8W 1206 RES SMT	1	R11	VENKEL
41	CR0603-16W-102JT	1 K 5% 1/16W 0603 RES SMT	2	R3, R9	VENKEL
42	CR0603-16W-330JT	33 OHM 5% 1/16W 0603 RES SMT	1	R12	VENKEL
43	CR0603-16W-243	24 K 5% 1/16W 0603 RES SMT	1	R15	VENKEL
44					
45					
46		CEBus 100-400 KHZ 12/12 TURN WITH HEADER	1	TX1	PER PRINT
47					
48	SSC P485	SSC, P485, PL TRANSCEIVER SO-20 IC	1	U2	INTELLON
49	SSC P111	SSC P111 PL MEDIA INTERFACE SO-16 IC	1	U1	INTELLON
50					
51	AS-12-20	12.000 MHZ CRYSTAL HC-49 US HALF CAN (20PF)	1	Y1	RALTRN

6. Power Line Node Regulatory Compliance Issues

6.1 Safety Certification

Network node devices connected to a DC power line or other communication medium may require listing with a certified testing laboratory (UL, CSA, etc.) to verify that they meet minimum safety requirements for marketability. Information regarding product classification and design/construction requirements is available from the appropriate agency.

6.2 Interference with Other Services

6.2.1 Federal Communication Commission Regulations

Radiated emissions from most types of electronic devices are stringently limited by Part 15 of the Federal Communications Commission rules. Communication devices based on Intellon's SSC technology are classified as "unintentional radiators". This type of digital device is described in Part 15 as "A device that intentionally generates radio frequency energy for use within the device, or that sends radio frequency signals by conduction to associated equipment via connecting wiring, but which is not intended to emit RF energy by radiation or induction".

Regulation of emissions under Part 15 depends on the nature of the communication system. For example, a P485-based twisted pair communication system used in a residential dwelling would be required to comply with radiated emission requirements of Part 15. On the other hand, the FCC currently exempts "A digital device utilized exclusively in any transportation vehicle including motor vehicles and aircraft" from the specific technical standards and other requirements contained in Part 15. However, the rules state that "it is strongly recommended that the manufacturer of an exempted device endeavor to have the device meet the specific technical standards in this part". The P485 system designer should consult Part 15 to determine applicability of the regulations to his specific application.

6.2.2 DC Power Line Applications and SAE Recommended Practices

Although compliance with FCC Part 15 regulations is not required for devices operated on tractor trailer systems, care should be taken to ensure that a power line communication system does not interfere with other services used on the vehicle. For this reason, the Society of Automotive Engineers has developed guidelines for conducted and radiated emissions due to devices operated on tractor/trailers. These guidelines and the associated measurement techniques are defined in the SAE recommended practice documents J551 and J1113.

P485 applications will fall under the requirements of J551/4, "Test Limits and Methods of Measurement of Radio Disturbance Characteristics of Vehicles and Devices, Broadband and Narrowband, 150 kHz to 1000 MHz" and J1113/41, "Limits and Methods of Measurement of Radio Disturbance Characteristics of Components and Modules for the Protection of Receivers Used On Board Vehicles". The radiation limits presented in these documents are designed to prevent interference to radio receivers used on the vehicle, including AM and FM broadcast receivers, television receivers, land-mobile radio receivers, radio telephone devices and amateur and citizens radio receivers.

6.2.3 Power Line Communication Device Measurement Tips

The SAE recommended practices outline measurements of power line conducted emissions using a Line Impedance Stabilization Network (LISN) and a Spectrum Analyzer or EMI Receiver. Measurement of conducted emissions should be made using the following guidelines.

1. The Spectrum Analyzer (EMI Receiver) should be configured as follows:

Resolution Bandwidth	9 kHz or 120 kHz as appropriate for frequency band
Video Bandwidth	Off
Detector	CISPR Quasi-peak
Other Settings	Within manufacturer's recommended calibration range.

2. The output level of SSC devices in the 100 to 400 kHz frequency range, when measured at the LISN port, will be greater than +105 dB μ V. The out-of-band limits for emissions described in J1113/4 are in the range of +20 to +80 dB μ V. Thus, if the analyzer reference level is set to a value of 80 dB μ V (or less) to obtain good measurement accuracy, the 105 dB μ V SSC signals will create intermodulation products in the front end of the spectrum analyzer. These intermodulation products will adversely affect the readings in the band of interest, although they might be outside the sweep range of the analyzer. High pass filters should be used at the analyzer input as follows:
 - To observe the SSC communication signal spectrum, the spectrum analyzer reference level should be set to 110 to 120 dB μ V and a 10 kHz high pass filter should be used at the analyzer input.
 - To measure out-of-band signals in higher frequency ranges, the analyzer reference level should be set to 80 dB μ V and a 450 kHz, 7 to 10 pole high pass filter should be used to avoid spectrum analyzer input overload protection.
 - Note: Do not rely on the spectrum analyzer's overload indicator. Intermodulation products are produced in most analyzers well before this indicator becomes active.
3. The LISN should be isolated from the DC power line source. A Low Pass Filter may be used to supply DC power to the LISN. Before making measurements, verify that there is no interference from the DC power source by observing the frequency band of interest with no devices connected to the LISN output.
4. The LISN should always be terminated properly. The typical test configuration contains two LISN devices, one on the "Line" side of the DC supply and one on the "Neutral" side of the supply. A 50 ohm spectrum analyzer input properly terminates the LISN being utilized. The unused LISN must be terminated in 50 ohms to avoid erroneous readings.



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